CLAIMS

1. A LSI layout method for a LSI design by automatic arrangement wiring of standard cells, comprising the operations of:

providing power supply capacitor cells as one of the standard cells in addition to logic gate cells provided as standard cells,

determining a capacitance value of the power supply capacitor cells so as to correspond to a drive load capacity value of the logic gate cells to which the power supply capacitor cells are to be arranged, and

arranging the power supply capacitor cells in the vicinity of the logic gate cells.

2. The LSI layout method according to claim 1, wherein the capacitance value of the power supply capacitor cells is determined to be substantially twice as large as the drive load capacity value of the logic gate cells.

3. The LSI layout method according to claim 1, wherein the power supply capacitor cells are arranged in the vicinity of the logic gate cells which change simultaneously with clock synchronization.

4. A LSI layout method for a LSI design by automatic arrangement wiring of standard cells, comprising the operations of:

providing power supply capacitor cells as one of the standard cells, and

arranging the power supply capacitor cells in spaces of each block where standard cells are not arranged by the automatic arrangement wiring.